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RM-6487

B. E. - II (Sem. IV) (ECC) Examination

May / June – 2010

Electronic Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 2 (Sem. 4) (ECC)

Name of the Subject :

☛ Electronic Circuits

☛ Subject Code No. : 6 4 8 7 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

(2) Figures on right side indicate full marks.

(3) Support your answer with neat sketches.

(4) Assume necessary data, if required.

(5) Write both sections in separate answer books.

SECTION - I

1 (a) Answer the short questions : **10**

(i) Why the channel of a JFET is never completely closed at drain end?

(ii) What is pinch off voltage of JFET?

(iii) How does FET behave for small value of V_{DS} and for large value of V_{DS}?

(iv) Why input impedance of FET is very high?

(v) Why are R-C coupled amplifier widely used as a voltage amplifier?

(vi) What is the effect of removal of emitter bypass capacitor in CE amplifier circuit?

(vii) What is miller effect?

(viii) Define F_T in context of high frequency model of a transistor.

(ix) What do you mean by alpha cut off frequency?

(x) Why source and drain are reversible in FET?

(b) As shown in figure 1, two FETs are connected in parallel. Show that the equivalent FET has 6

$$\frac{1}{rds} = \frac{1}{rds_1} + \frac{1}{rds_2} \quad \text{and} \quad \mu = \frac{\mu_1 rds_2 + \mu_2 rds_1}{rds_1 + rds_2}$$

Show that effective gm is doubled and rds is halved and μ remain same if both FETs are identical.

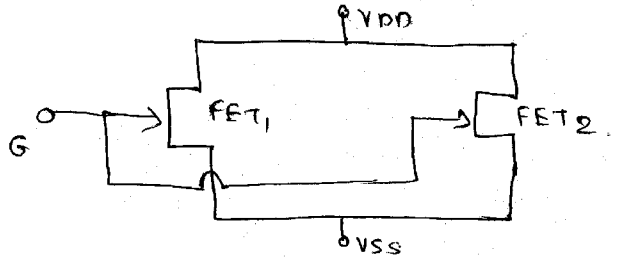


Figure 1

(c) Mention different biasing techniques for FET and explain self bias technique in brief. 4

2 Attempt any two : 16

(a) Derive the equation for gain in the case of common emitter configuration while considering the effect of emitter bypass capacitor.

(b) For the source follower circuit shown in figure 2, sketch asymptotic voltage gain for low frequency. Also find lower 3-dB frequency gm = 2mS, rds = 15 kΩ.

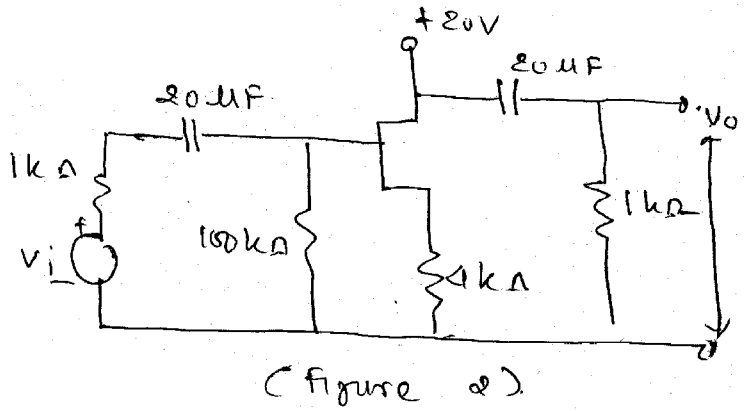
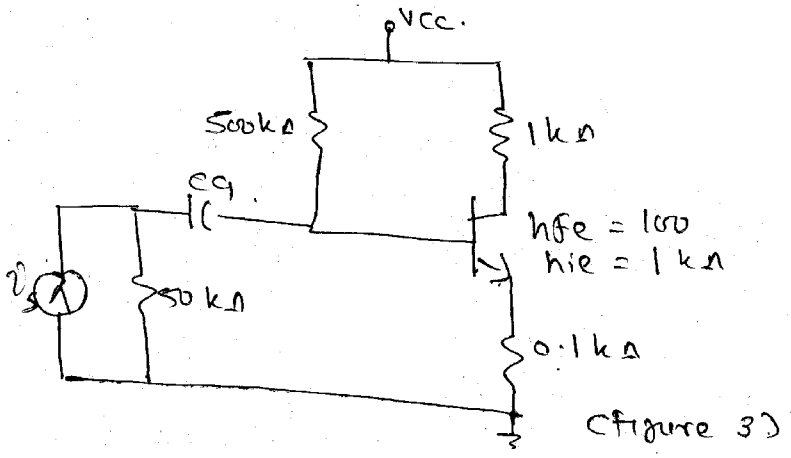


Figure 2

(c) Find and plot transfer function v_o/i_s for amplifier shown in figure 3. Also find C_q such that lower 3dB frequency is at 10 rad/sec.

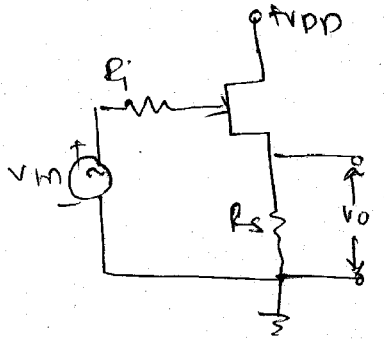


(Figure 3)

3 Attempt any **two** : **14**

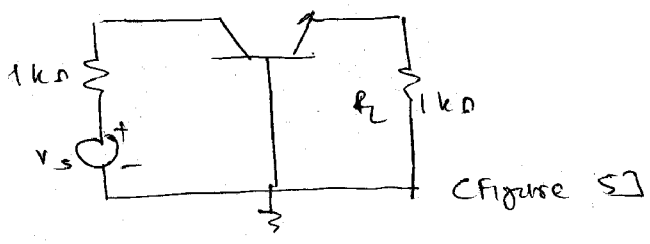
(a) Explain emitter follower at high frequency. Derive the expression for voltage gain and high frequency.

(b) The source follower shown in figure 4. The JFET of shown figure 4 has following parameters gm = 3mA/V, C_{gd} = 0.2 PF, C_{gs} = 20 PF, R_i = 10 KΩ, R_s = 2 kΩ. Find the upper 3dB frequency and plot asymptotes for voltage gain $|v_o/v_{in}|$.



(Figure 4)

(c) For common base amplifier shown in figure 5, plot asymptotic magnitude plot for (v_o/v_i) and indicate upper 3-dB cut off frequency with h_{fe} = 50, rb'e = 1 kΩ, cb'e = 40 PF, cb'c = 1 PF.



(Figure 5)

SECTION - II

4 (a) Answer following questions :

(i) Enlist advantages of negative feedback. **3**

(ii) Determine the voltage gain, input and output impedance with feedback for voltage series feedback having **3**

$A = -100$, $R_i = 10\,k\Omega$, $R_o = 20\,k\Omega$ for feedback of $\beta = -0.1$

(iii) Define : Gain margin and Phase margin. **4**

(b) (i) Explain RC phase shift oscillator. **5**

(ii) Find the Gain Bandwidth (GBW) product of a JFET amplifier having the parameters : **5**

gm = 3 mS, C_{gs} = 6 PF, C_{gd} = 2 PF,

r_{ds} = 70 kΩ and R_d = 10 kΩ.

5 (a) Explain : Synchronously tuned amplifier. **8**

(b) Draw and explain current shunt feedback circuit with necessary equations. **7**

OR

5 (a) What is Barkhausen criterion for oscillation? Explain in detail. **7**

(b) What is the effect of feedback connection on input and output impedance for voltage series and current series connections. Explain with derivations. **8**

6 Write short notes on any **three** : **15**

(i) Colpitt oscillator

(ii) Single tuned amplifier

(iii) Nyquist criteria

(iv) Effect of negative feedback on gain and bandwidth.
